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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,637	01/20/2004	Raghavan Sudhakar	ITL.1490US (P16291)	3339

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EXAMINER
FOTAKIS, ARISTOCRATIS

ART UNIT	PAPER NUMBER
2611	

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11/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,637	SUDHAKAR, RAGHAVAN	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after t he mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/09/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3, 7 - 19, 21 and 23 - 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 7 - 19, 21 and 23 - 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 7, 9, 11 – 15, 18 – 19, 21, 24 and 26 – 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamanaka et al. (US 6,330,684).

Re claims 1 and 18, Yamanaka teaches of an apparatus (Fig.6) comprising: means for storing 2^{n-1} branch metric values (2 branch values, 00 or 01 or 10 or 11, n = 2, Fig.7, Col 5, Lines 40 - 57) to be used in a 1/n rate signal decoder (rate ½, Fig.7) to a storage device (#3, Fig.6); means for loading from the storage device no more than the 2^{n-1} branch metric values to generate 2^{k-1} signal states for each of an n-bit signal value received by a communications signal decoder (Col 1, Lines 23 – 39), wherein K is a constraint length corresponding to a number of decoder state Variables corresponding to the n-bits; means for performing 2^{k-2} add, compare, select (ACS) butterfly calculations corresponding to the no more than 2^{n-1} branch metric values (Col 40, Lines 35 – 52), including means for evaluating two path metrics in parallel (Abstract, Fig.14

and Col 2, Lines 53 – 67) responsive to a single vector add-subtract instruction to operate on two prior path metrics and stored branch metrics (Col 2, Lines 53 – 64, Fig.9), and a single VITMAX instruction to compare the upper and lower bit values of two registers and store the two larger values in a third register (Col 2, Lines 65 – 67 to Col 3, Lines 1 – 7 and Col 6, Lines 33 - 40 and Lines 60 – 65, Figs.9 and 14).

Re claim 19, Yamanaka teaches of the storage unit is at least one memory location and the loading unit is a memory interface unit (#4, BUS, Fig.14)

Re claims 3 and 21, Yamanaka teaches of performing 2^{k-2} ACS butterfly calculations comprising digital signal processor (DSP) registers (#16, #17, Fig.14) and accumulators (Fig.14) (Fig.14, Lines 1 - 11) being used in 16-bit computation mode (*dual 16-bit mode* ,Col 2, Lines 53 – 55).

Re claims 7 and 24, Yamanaka teaches of the instruction storing two decision bits (path select signal) into an accumulator (ACS) in order to allow a selected path metric to be tracked (trace-back, Col 15, Lines 5 – 9).

Re claims 9 and 26, Yamanaka teaches of a method to perform a Viterbi decoding algorithm comprising: initializing path metric buffers (#1, Fig.14) and trace back buffers (always required in a Viterbi decoder in order to perform a traceback on the set of accumulated path decisions); evaluating branch metric (BM) kernel equations (Col 2, Equation 2); storing the result of the BM evaluations (#3, Fig.14); performing path metric evaluations corresponding to each BM evaluation (#5 – #8, Fig.14) (Col 3, Lines 54 – 61), the path metric evaluations using a single vector add-subtract instruction to operate on two prior path metrics and two stored BMs and a single vector compare-select instruction to compare upper and lower portions of first and second register values, respectively, and to store the larger of the respective upper and lower portions in a third register and store two decision bits into an accumulator (see rejection of claims 1 and 18).

Re claims 11, Yamanaka teaches of performing add, compare, and select (ACS) calculations to determine a most probable next state transition for each current state of an input signal to the Viterbi decoding algorithm (Fig.14, Col 3, lines 54 – 61).

Re claims 12 and 27, Yamanaka teaches of determining a maximum path metric values corresponding to the path metric evaluations and storing them (trace-back, Col 1, Lines 19 – 22, Col 15, Lines 6 - 9).

Re claims 13 and 28, Yamanaka teaches of tracing back through state transitions to determine the minimum path between each bit state decoded by the Viterbi decoding algorithm (trace-back, Col 1, Lines 19 – 22, Col 15, Lines 6 - 9).

Re claims 14, Yamanaka teaches of the number of BM equations to be no more than 4 (BM0 – BM4, Fig.7).

Re claims 15, Yamanaka teaches of the ACS calculations comprising the BM calculations and path metric calculations for each current state (Fig.8, Fig.14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka.

Yamanaka teaches all the limitations of claim 9 as well as means for evaluating two path metrics in parallel (Fig.14) comprising an instruction (Col 9, Lines 19 – 27, Fig. 15) to compare the upper and lower bit values (#5 and #9, Fig.14) of two DSP registers (#16, #17) and store the two larger values in a third register (#14, Fig.14). The applicant uses in his invention embodiments a constraint length of K=4 and a code rate of ½ (Col 7, Lines 10 – 16). However, Yamanaka cites that the invention can perform equally well by using other values obtaining the same advantages as the embodiment taught (Col 7, Lines 16 – 20).

Therefore it would be obvious to one of ordinary skill in this art to modify the invention of Yamanaka to obtain the invention as specified in the claim.

Claims 8 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Leisbon ("Tailored Processors Hit Closer to performance Aims" June 2003, COTS Journal).

Yamanaka teaches all the limitations of claims 7 and 24 except of the ACS butterfly calculations to be performed within two DSP processing cycles.

Leisbon discloses a Viterbi decoder performing butterfly computations across two cycles occurring in parallel with a load operation for a subsequent butterfly and a store operation for a prior butterfly (Page 45, Col 3, Lines 1 – 7 to Page 46, Col 1, Lines 1 – 4)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have performed butterfly computations across two DSP cycles to save hardware and to match the computational and data transfer resources (Page 46, Col 1, Lines 1 – 4).

Claims 16 – 17 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Zhong et al (US 5,970,104).

Yamanaka teaches all the limitations of claim 11 except of the ACS calculations comprising path metric calculations and not BM calculations for each current state.

Zhong teaches of a Viterbi decoder generating a branch metric table from first and second data signals taken at two sample times and provides selected branch metrics to an add/compare/select circuit in response to branch indices from a branch index generator (Abstract). The branch index generator (#112, Fig.1) selects for each possible previous state (#202, Fig.2), a branch metric λ indicative of the branch transition from the previous state (#202) to the current state (#204) from the branch metric table (#120, Fig. 1). The Viterbi decoder then calculates, for each possible previous state, a state metric, which is the sum of the state metric of the previous state and the branch metric λ of the branch transition from such state to the current state. Each current state thus has a candidate state metric for each possible previous state (#202) to the current state (#204) (Col 3, Lines 39 – 47). By making this branch selection at each data time, instead of recalculating the path before the previous state, the Viterbi decoder 104 performs less calculations (Col 4, Lines 10 – 14).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to not have calculated the branch metrics for each state for the benefit of less complexity.

Response to Arguments

Applicant's arguments filed October 9, 2007, have been fully considered but they are not persuasive.

Applicant submits that Yamanaka nowhere teaches that two path metrics are evaluated in parallel responsive to a single vector add-subtract instruction and VITMAX instruction where multiple instructions are issued, one in each cycle. The Applicant further submits that while these instructions may execute in parallel as described in Yamanaka, these operations are not according to a single vector add-subtract instruction and a single VITMAX instruction.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (the cycle comparison of the Applicant invention compared to the patent of Yamanaka on the number of instructions used) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER